UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,940	06/08/2004	Jui-Meng Jao	NAUP0480USA	3939

27765 7590 10/04/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,940	JAO ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 3, 5 – 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Owada et al. (US Patent 5220199).

3. Owada et al. teach a parasitic capacitance-preventing dummy solder bump structure (col. 5 lines 44 – 49), the dummy solder bump structure being formed on a substrate, the dummy solder bump structure comprising:

at least one conductive layer (3) formed on the substrate; a dielectric layer (5) formed on the substrate to cover the conductive layer; an under bump metallurgy (UBM) layer (30) formed on the dielectric layer; and a solder bump (2) formed on the UBM layer.

wherein the substrate is a semiconductor wafer with circuits formed inside the semiconductor wafer (fig. 4), the dielectric layer comprises at least one deposition layer formed by a chemical vapor deposition (CVD) process and employed as a passivation layer (col. 10 line 44), and the deposition layer comprises either silicon nitride or silicon oxide (col. 7 line 26);

wherein a plurality of solder bump structures is formed on the dielectric layer (fig. 6); and

wherein each of the solder bump structures comprises a metal pad formed on the dielectric layer, and an UBM layer formed on the metal pad, and a solder bump formed on the UBM layer (col. 7 lines 26 – 43).

4. Claims 1, 2, 4 – 11, 13 – 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (AAPA).

5. AAPA (fig. 4) teach a method of forming a solder bump on a substrate, the substrate comprising at least one conductive layer positioned on a surface of the substrate, the surface of the substrate comprising a first area and a second area, the method comprising:

performing a CVD process to form a dielectric layer (18) on the substrate to cover the conductive layer (16);

forming at least one via plug (22) in portions of the dielectric layer within the first area down to a surface of the conductive layer;

forming at least one metal pad (24) electrically connected to the via plug;

performing an UBM process tot form at least one UBM layer (28) to cover both the metal pad (24) within the first area and portions of the dielectric layer (26) within the second area;

forming a solder bump (30) on the UBM layer;

wherein the dielectric layer comprises a passivation layer (26) atop the dielectric layer;

wherein the via plug comprises either one of titanium (Ti), titanium nitride (TiN), tungsten (W), aluminum (Al), copper (Cu) or copper-aluminum alloy (paragraph 6);

wherein the UBM layer is formed by a sputtering process (paragraph 7);

wherein the substrate is a semiconductor wafer with circuits formed inside the semiconductor wafer (paragraph 5);

wherein the first area and the second area are respectively a central area and a border area of the surface of the substrate (paragraph 5); and

wherein the solder bump formed within the second area is employed as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes (paragraph 7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. (US Patent 5220199) in view of Viswanadam et al. (US Patent 6759319).

9. Owada et al. teach the features previously outlined, but lack a UBM metal layer formed by a sputtering process.

10. However, Viswanadam et al. teach a UBM metal layer formed by a sputtering process (col. 2 lines 54 – 57) to provide a solder bumping free of residue.

11. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Viswanadam et al. into the Owada et al. reference to improve bump-contact performance.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owada et al. (US Patent 5220199) in view of Ishikawa et al. (JP Patent 2003017530).

13. Owada et al. teach the features previously outlined, but lack wherein the solder bump formed within the second area is employed as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

14. However, Ishikawa et al. teach wherein the solder bump formed within the second area is employed as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes (abstract).

15. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Ishikawa et al. into the Owada et al. reference to achieve a laminar flow of underfill material.

16. Claims 3, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view Owada et al. (US Patent 5220199).

17. AAPA teaches the features previously outlined, but lacks the dielectric layer and the passivation layer comprising either silicon nitride or silicon oxide.

18. However, Owada et al. teach dielectric layer and the passivation layer comprising either silicon nitride or silicon oxide (col. 7 line 26).

19. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Owada et al. into the AAPA as art recognized equivalents.

20. Prior art considered, but not used in the rejection include Loo et al. (US Patent 6118180), and Sullivan et al. (US Patent 6333557).

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2825

IA

September 29, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800